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10/569,825	02/01/2007	Marcel Lapointe	OBL-007-US	5375

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EXAMINER

HUANG, DAVID S

ART UNIT	PAPER NUMBER
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2611

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/569,825	Applicant(s) LAPOINTE, MARCEL	
	Examiner DAVID HUANG	Art Unit 2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 February 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-7 and 9-12 is/are rejected.
- 7) ☒ Claim(s) 8 and 13 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 February 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Objections

1. **Claims 1-3 and 13** are objected to because of the following informalities:

Claim 1, line 6, recites "an FIR filter" which should be --the FIR filter-- to refer back to the FIR filter recited on line 1.

Claims 2-3 are dependent on claim 1.

Claim 13, line 9, recites "networkfor" which should be --network for-- to correct a typographical error.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. **Claims 11 and 12** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding **claim 11**, the preamble text recites "data bits that are shifted through delay elements at a reference clock rate" on lines 1-2, but i) recites a conflicting limitation, "data bits that are shifted through delay elements... at a shift rate that is a sub-multiple Q of the reference clock rate." It is unclear whether the intended shift rate is the reference clock rate or the sub-multiple Q of the reference clock rate. For examination on the merits, the claim will be interpreted as best understood.

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Regarding **claim 12**, the preamble text recites "data bits that are shifted through delay elements at a reference clock rate" on lines 2-3, but i) recites a conflicting limitation, "data bits... operating at a shift rate that is the quotient of the reference clock rate divided by Q." It is unclear whether the intended shift rate is the reference clock rate or quotient of the reference clock rate divided by Q. For examination on the merits, the shift rate will be interpreted as the quotient of the reference clock rate divided by Q.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 1-6 and 11** are rejected under 35 U.S.C. 102(b) as being anticipated by Lee et al. (US 6,138,132).

Regarding **claim 1**, Lee et al. discloses an apparatus for use in a reduced clock finite impulse response (FIR) filter comprising:

i) a multiplexer/multiplier (mux/mul) means having Q inputs and one output (MUX 211, 221, Fig. 2);

ii) selection means for controlling said mux/mul means operative to produce said one output from one of said Q inputs (waveform generator 73, Fig. 2); and

iii) output conditioning means coupled to the output of said mux/mul means to produce a conditioned output signal corresponding to a coefficient used in an FIR filter (ROM 311, 321,

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Fig. 2; ROM based FIR filter, col. 3, lines 11-14, filter coefficients, col. 6, lines 1-8; see also col. 1-2 for background on filter coefficients).

Regarding **claim 2**, Lee et al. further discloses said signal conditioning means modifies the gain and the sign of the output of the corresponding mux/mul (gain inherently modified by filter coefficients, col. 1, line 50 - col. 2, line 20; and inverting output from the ROM, computing 2's complement, "sign", col. 5, lines 15-27, block 611, Fig. 2).

Regarding **claim 3**, Lee et al. further discloses means to produce a clock signal at the data rate of a data signal coupled to said selection means wherein said clock signal controls the selected output of said selection means from one of said Q inputs (clock, Figs. 2 and 5, coupled to Waveform generator 73, Fig. 2; outputting MSEL to MUXes 211 and 221, Fig. 2).

Regarding **claim 4**, Lee et al. discloses an apparatus for use in a reduced clock rate finite impulse response filter comprising:

i) Q latch means all coupled to an input data signal having a unit interval rate and each latch means providing a latched output signal in response to a latch control signal (two shift registers 101 and 111, Fig. 2);

ii) Q multiplexer/multiplier (mux/mul) means, each mux/mul means providing one output and Q inputs to receive the latched output signal of a respective latch means (two MUXes 211 and 221, Fig. 2); and

iii) selection means for controlling said mux/mul means operative to produce an output signal selected from one of said Q inputs (Waveform Generator 73, outputting MSEL to control MUXes, Fig. 2)

Regarding **claim 5**, Lee et al. further discloses

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i) signal conditioning means for each mux/mul means to condition the output signal of the mux/mul means (ROMs 311 and 321, XOR 601 and 2's Complement block 611, Fig. 2); and

ii) summing means to sum the conditioned signals of all such signal conditioning means (Adder 401, Fig. 2).

Regarding **claim 6**, Lee et al. further discloses said signal conditioning means modifies the gain and the sign of the output signal of the corresponding mux/mul means (gain inherently modified by filter coefficients, col. 1, line 50 - col. 2, line 20; and inverting output from the ROM, computing 2's complement, "sign", col. 5, lines 15-27, block 611, Fig. 2).

Regarding **claim 10**, Lee et al. discloses the selection means operates to select an output signal from one of said Q inputs at a rate corresponding to the unit interval rate of said input data signal (same MSEL clock signal used to control MUXes 211 and 221 are also to clock shift registers 101 and 111).

Regarding **claim 11**, Lee et al. discloses in a transversal finite impulse response (FIR) filter for processing data bits that are shifted through delay elements at reference clock rate and each delay element is coupled to a corresponding multiplier and all of the multiplied outputs are summed, the improvement comprising:

i) a column of delay elements arranged to form Q rows for processing data bits that are shifted through delay elements of each row at a shift rate that is a sub-multiple Q of the reference clock rate (Shift registers 101, 111, Fig. 2; shifted according to MSEL);

ii) Q multiplexer/multiplier (mux/mul) means having Q inputs each correspondingly coupled to a delay element in said column of delay elements and each said mux/mul produces one output from one of said Q inputs (MUXes 211 and 221, Fig. 2); and

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iii) selection means for controlling said mux/mul means operative to select said one output of said Q inputs at said reference clock rate (waveform generator 73 at MSEL, Fig. 2), wherein said selected output of a mux/mul is provided to the corresponding multiplier (ROMs 311 and 321, XOR 601, and 2's Complement 611, Fig. 2) and summed (Adder 401, Fig. 2) in the transversal FIR filter (FIR filter, col. 3, line 11).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. **Claims 7 and 9** are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (US 6,138,132) in view of Lewis et al. (US 5,452,324).

Regarding **claim 7**, Lee et al. discloses everything applied to claim 4, and further discloses i) means to produce a clock signal (implicit in "clock" input to 713, Fig. 5).

Lee et al. fails to expressly disclose Q phase delay means coupled to said clock signal providing an output latch control signal to a corresponding latch means.

Nevertheless, Lee et al. discloses two input data are crossingly selected to change the data inputted into the first and second ROMs 31 and 32 (col. 5, lines 49-56, Fig. 2).

Lewis et al. discloses a delay locked loop circuit (Fig. 3) that phase delays a reference clock signal to output different phase delayed signals, used for the clock inputs of flip flops

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(phase delayed signal 5 and 10, col. 8, lines 12-23). This places each sample point half-way between the transition points of incoming data 24 (col. 8, lines 21-23).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide Lee et al. with the phase locked loop circuit of Lewis et al., since it provide greater adjustability in clock phase timing and improves performance by placing sample points halfway between the transition points of incoming data.

Regarding **claim 9**, Lee et al. discloses everything applied to claim 7, and further discloses the means to produce a clock signal operates to produce a clock signal that is a sub-multiple Q of the unit interval rate of said input data signal (MSEL is a four-divided clock signal of the clock signal CLOCK, col. 5, lines 49-53, Fig. 5, Fig. 2).

Allowable Subject Matter

8. **Claim 8** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. **Claim 13** is objected to, but would be allowable if rewritten or amended to address the formal matters.

10. **Claim 12** would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID HUANG whose telephone number is (571)270-1798.

The examiner can normally be reached on Monday - Friday, 8:00 a.m. - 5:00 p.m., EST.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on (571) 272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DSH/dsh
9/22/2009
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Examiner, Art Unit 2611
/Shuwang Liu/
Supervisory Patent Examiner, Art Unit 2611